REMARKS

Claims 1-20 are pending in this application. Claims 1, 6, 8, 9, 12, and 13 are amended. New claims 16-20 are added. In the Office Action, claims 1-14 are rejected over prior art. Reconsideration of the rejection is respectfully requested.

CLAIM REJECTION UNDER 35 U.S.C. §112

Claim 9 is amended to remove the Examiner's rejection. No new matter has been added by the amendment.

CLAIM REJECTION UNDER 35 U.S.C. §102

Claims 1, 8, and 12-14 are rejected under 35 U.S.C. § 102(b), as being anticipated by Jeng et al. (U.S. Patent 6,097,199). The rejection is respectfully traversed.

Applicants respectfully submit that the Examiner has mischaracterized Jeng et al. vis-à-vis in rejecting the present claims. Jeng et al. discloses a test board capable of testing different semiconductor packages with various pin numbers. Specifically, a universal decoder test board (UDTB) is disclosed by "providing an interface capable of coupling a package of a given type regardless of the pins its has [sic]." Column 4, lines 39-44. Details of the interface are disclosed throughout the specification. In other words, a single UDTB is sufficient to test different semiconductor packages with various pin numbers. However, the test board of Jeng et al. still requires different tester interface boards to test semiconductor packages with different manufacture testers. Column 2, lines 19-23; column 3, lines 48-52; and column 4, lines 56-58: ("A tester board specifically adapted to interface with a tester for a particular manufacture's hardware.")

Example embodiments of the present invention, and as recited in the claims, specifically disclose a test board (mother board) electrically compatible with each of respective test heads of different testers. In other words, not only is the test board of the example embodiments of the present invention capable of testing different semiconductors with various pin numbers, it may also be compatible with each of respective test heads of different testers.

The single test board of the example embodiments of the present invention is capable of testing all semiconductor packages with different testers. Jeng et al. requires a separate tester interface for each separate tester manufacturer.

The Applicants respectfully submit that Jeng et al. fails to disclose each and every feature of independent claims 1, 8 and 15, therefore, it cannot provide a basis for rejection under 35 U.S.C. §102. Accordingly, the Applicants submit that claims 1, 8, and 12-14, are allowable over the prior art. Withdrawal of the rejection is respectfully requested.

CLAIM REJECTION UNDER 35 U.S.C. §103

Claims 2-7 and 9-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Jeng et al. in view of Applicants admitted prior art. This rejection is also respectfully traversed.

Even if the APA discloses that a mother board provides signal paths for mixed signals, Jeng et al. neither discloses nor suggests the claimed invention as recited in amended independent claims 1 and 8. Claims 2-7 and 9-11, which depend on claims 1 and 8, respectively, are distinguished over the Examiner's cited references individually and in combination thereof. Reconsideration and withdrawal of the rejection is respectfully requested.

Newly added independent claim 15 recite common features of independent claims 1 and 8; therefore, Applicants respectfully submit that claim 15 and dependent claims 16-19 are patentable for the same reasons given above.

CONCLUSION

In view of the above remarks, reconsideration of the rejections and allowance of claims 1-4 and 6-19 are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If the Examiner believes that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 668-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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